REMARKS

Favorable reconsideration and allowance of the subject application are respectfully requested. Claims 1-4 and 6-13 are pending in the present application, with claims 1 and 2 being independent.

Claim Rejections Under 35 U.S.C. §103

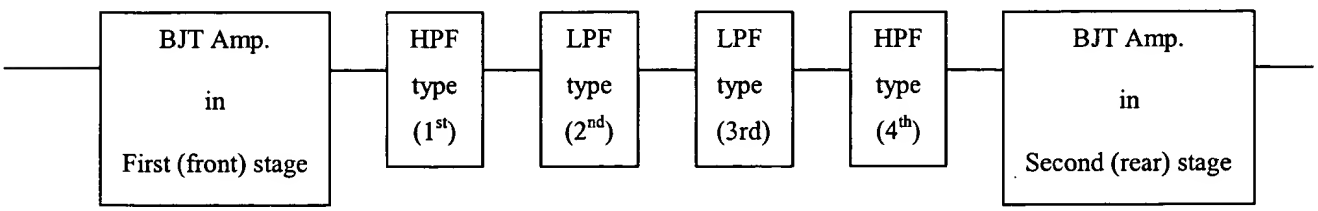
The Examiner rejected claims 1-4 and 6-13 under 35 U.S.C. §103(a) as being unpatentable over *Mizan* et al. (US Patent No. 5,339,047). This rejection is respectfully traversed insofar as it pertains to the presently pending claims.

Mizan et al. is directed to a bipolar junction transistor (BJT) amplifier and matching networks. Referring to Fig. 1 of *Mizan* et al. there is shown a configuration in which a BJT, an input matching network, and an output matching network are connected in series. The input matching network (as a first combination matching circuit), consisting of a LPF (Low Pass Filter) type and a HPF (High Pass Filter) type, is connected to the input section of the BJT amplifier. The output matching network (as a second combination matching circuit), consisting of a LPF type and a HPF type, is connected to the output section of the BJT amplifier. Although not shown in FIG. 1 of *Mizan*, but shown in FIG. 5 schematically, are

two adjacent BJT amplifiers, functioning as a multistage amplifier, which are connected through four matching circuits (not shown clearly in the figures of *Mizan* et al.), namely, the first combination matching circuit (consisting of two matching circuits) and the second combination matching circuit (consisting of two matching circuits).

In the configuration of *Mizan* et al. a connection of two BJT amplifiers (first and second stage BJT amplifiers or elements) in series must require the use of two combination matching circuits (each consists of two matching circuits). The first *combination matching* circuit consisting of a combination of LPF type and HPF type is connected to the output side of the first (or front) stage BJT amplifier. The second combination matching circuit consisting of a combination *of* LPF type and HPF type is connected to the input side of the second (or rear) stage BJT amplifier. That is, the connection of the adjacent BJT amplifiers in series requires the use of the following four matching circuits connected *in* series, as shown in the following diagram 1).

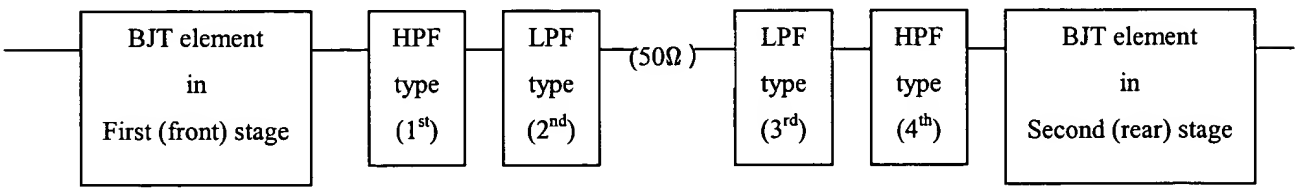
Diagram 1 <*Mizan's* configuration>



In contrast thereto, independent claims 1 and 2 both recite that "a matching circuit, [is] directly connected between each pair of amplifying elements [that are] adjacent to each other." In other words, in *Mizan's* configuration, as shown above, cannot be directly connected between each pair of amplifying elements. Therefore, *Mizan* et al. fails to anticipate the presently pending claims.

Additionally, in the configuration of the multistage amplifier of *Mizan* et al., the first (or front) and second (or rear) BJT amplifiers are connected in series through the first to fourth matching circuits (see above Diagram 1), and the second matching circuit must be connected to the third matching circuit with the impedance of 50Ω. That is, as described above, when the four stage matching circuits are placed between the first and second BJT amplifiers, which are adjacent to each other, the impedance between the second and third matching circuits must be set to the value of 50Ω, which is shown further below in Diagram 2.

Diagram 2 <*Mizan's* configuration>



HBT:Hetero junction Bipolar Transistor

On the contrary, according to the present invention, and as shown in FIG. 3, only the two matching circuits 28 and 29 (not four matching circuits as in *Mizan* et al.) are placed between the adjacent amplifiers 23 and 24. Therefore, the magnitude of the impedance between the two matching circuits 28 and 29 can be set to a value between the impedance of the first (front) stage amplifier 23 and the impedance of the second (rear) stage amplifier 24.

In other words, the present invention is different in configuration and function from *Mizan et al.* In *Mizan et al.*, adjacent amplifiers are matched using a characteristic impedance of the matching circuit.

On the contrary, the present invention uses an impedance value between the output impedance of the first (front) stage amplifier and the input impedance of the second (rear) stage amplifier connected to the first stage amplifier. This configuration of the present invention can obtain a low strain and a matching between different stages with high efficiency. *Mizan's* configuration can not obtain the effects of the present invention.

Dependent claims 3-4 and 6-13 should be considered allowable at least for depending from an allowable base claim. Accordingly,

Applicants respectfully request that the Examiner withdraw the rejections.

Conclusion

In view of the above amendments and remarks, this application appears to be in condition for allowance and the Examiner is, therefore, requested to reexamine the application and pass the claims to issue.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Martin Geissler (Reg. 51,011) at telephone number (703) 205-8000, which is located in the Washington, DC area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees

required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachments: Version With Markings To Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES

In the Claims:

1. (Twice Amended) A multistage amplifier, comprising:

a plurality of amplifying elements for amplifying an input signal stage by stage and outputting an amplified signal; and

a matching circuit, [arranged] directly connected between each pair of amplifying elements adjacent to each other, for performing an impedance matching between the pair of amplifying elements, wherein [one of] the matching circuit [circuits] comprises:

a one-stage high pass filter type matching unit having a parallel inductor and a serial capacitor; and

a one-stage low pass filter type matching unit serially connected with the one-stage high pass filter type matching unit.

2. (Twice Amended) A multistage amplifier, comprising:

a plurality of amplifying elements for amplifying an input signal stage by stage and outputting an amplified signal; and

a matching circuit, [arranged] directly connected between each pair of amplifying elements adjacent to each other, for performing an impedance matching between the pair of amplifying elements, wherein the matching circuit arranged between the final-stage

amplifying element and the amplifying element placed just before the final-stage amplifying element comprises:

a one-stage high pass filter type matching unit having a parallel inductor and a serial capacitor; and

a one-stage low pass filter type matching unit serially connected with each other.